Q.P. Code:16EC424 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech III Year II Semester Supplementary Examinations July-2021

DIGITAL IC APPLICATIONS

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	a	Draw the circuit diagram of basic CMOS gate and explain its operation?	7M
	b	Compare CMOS, TTL and ECL logic families.	5M
		OR	
2	a	Design a 2-input NAND gate using diode logic and a transistor inverter. Analyze the circuit with the help of transfer characteristics.	6M
	b	Explain the following terms with reference to TTL gate. i) D.C noise margin ii) Logic levels	6M

UNIT-II

3	a	Explain the behavioral design elements of VHDL.	6M
	b	Design the logic circuit and write VHDL program for the following function. $F(X) = \Sigma A, B, C, D (0, 2, 5, 7, 8, 10, 13, 15) + d (1, 6, 11)$.	6M
		OR	
4	a	Explain about functions and procedures with an example.	6M
	b	Explain about VHDL program structure.	6M

UNIT-III

5	a	Design a 4 to 16 decoder with 74×138 IC's.	6M
	b	Write a VHDL program for the above design.	6M
		OR	
6		Design the following functions using PAL and PLA. i) $F_1 = \Sigma(0,1,2,5,7,11,13,14) + d(4,8,10)$ ii) $F_2 = \Sigma(0,3,5,6)$	12M

UNIT-IV

7	a	Design a self-correcting 4 bit, 4 state ring counters with a single circulating 0 using 74x194.	8M
	b	What do you mean by self-correcting counter.	4M
		OR	
8	a	Design a 4-bit Ring Counter and explain its operation.	6M
	b	Write a VHDL code for the above design.	6M

UNIT-V

9	a	Distinguish between latches and flip flop .Show the logic diagram for both. Explain the operation with the help of function table.	6M
	b	Write a VHDL code for a D-flip flop in behavioral model.	6M
		OR	
10		Design a 8-bit barrel shifter using three control inputs. Write a VHDL program for the same in data flow style	12M

*** END ***